PATENT ABSTRACTS OF JAPAN

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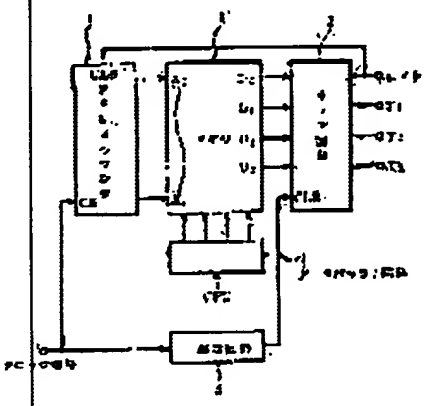
(54) TIMING GENERATING CIRCUIT

(57)Abstract:
PURPOSE: To extract plural pulses within a single rate by using the output of an address counter as the address input of a memory to read the data out of the memory and clearing the address counter by the rate output.
CONSTITUTION: The necessary data are written into a memory 2 from a CPU via a data buffer circuit 4. Then an address counter 1 is started with clock control. Thus the counter 1 starts increment. The output of the counter 1 is connected to the address input of the memory 2. The memory 2 sends its stored data to a latch circuit 3 as an output in parallel with the counting action of the counter 1. The circuit 3 latches the received data and the output rate of the circuit 3 is connected to the clear terminal of the counter 1. A delay circuit 5 supplies a clock signal for correction to the circuit 3 in the same timing as that of the signal received via the counter 1 and the memory 2. In such a way, the counter 1 is cleared by the rate output and therefore plural timing waveforms of different repeating cycles can be easily taken out.



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